Please replace paragraph [0008] with the following amended paragraph:

[0008] According to the claimed invention, a semiconductor package is provided. The

semiconductor package positioned on a first substrate includes a second substrate having

a first surface and a second surface, a chip positioned on the first surface of the second

substrate, a plurality of first bonding balls positioned on the second surface of the second

substrate and arranged in a line single row along a first direction for connecting the

second substrate to the first substrate, and at least a dummy bonding bar positioned on the

second surface of the second substrate for connecting the second substrate to the first

substrate and preventing the semiconductor package from inclining to one side. In

addition, the dummy bonding bar and the first bonding balls are arranged in the same

row.

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Please replace paragraph [0020] with the following amended paragraph:

[0020] Please refer to Fig.4 to Fig.6. Fig.4 is a bottom view of a semiconductor package

according to the first embodiment of the present invention. Fig.5 is a cross-sectional view

along line 5-5" of Fig.4.Fig.6 is a cross-sectional view along line 6-6" of Fig.4. As shown

in Fig.4 and Fig.5, a semiconductor package 30 includes a substrate 32 having an upper

surface 32a and a lower surface 32b, a chip 34 positioned on the upper surface 32a of the

substrate 32, a plurality of bonding pads 38 positioned on the lower surface 32b of the

substrate 32, and a plurality of bonding balls 36 respectively positioned on the bonding

pads 38. The semiconductor package 30 has only has a single rows of bonding pads 38

placed on the lower surface 32b of the substrate 32. The chip 34 is an image senor chip,

such as a CCD or a CMOS image sensor chip, and the chip 34 can be connected to the

substrate 12 by using a wiring bonding method or a flip-chip method. Additionally, the

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chip 34 has a rectangular shape, the bonding balls 36 are arranged in a line along a long side of the chip 34, and a length of a short side of the chip 34 is less than 1000 μ m. The substrate 32 can be a build-up printed circuit board, a co-fired ceramic substrate, a thin-film deposited substrate or a glass substrate.